ADM-PCIE-9V5
User Manual

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1 Introduction

The ADM-PCIE-9V5 is a high-performance reconfigurable computing card intended for Data Center applications, featuring a screened Xilinx Virtex UltraScale+ Plus FPGA with low latency transceivers and four QSFP-DD cages.

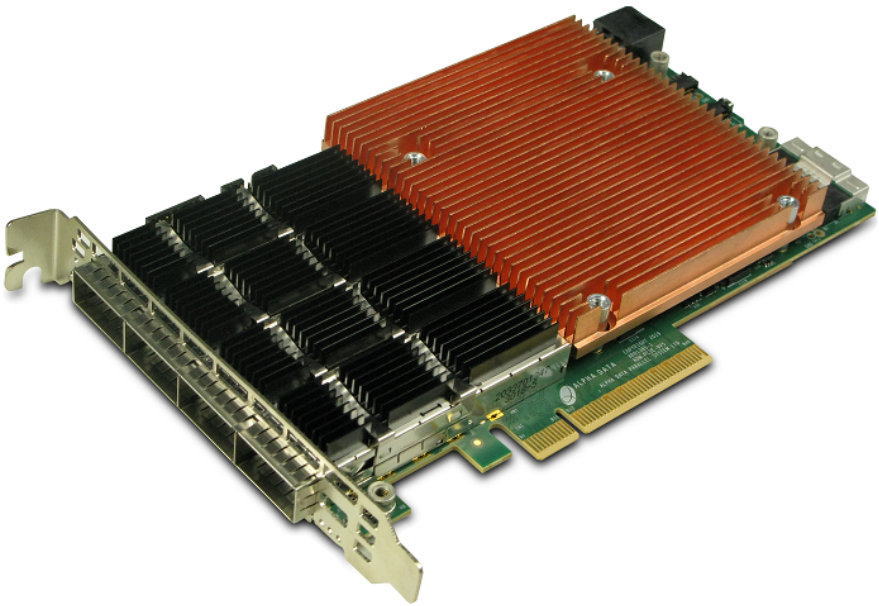

Figure 1 : ADM-PCIE-9V5 Product Photo

1.1 Key Features

Key Features

- PCIe Gen3 x8 capable
- Passive and active thermal management configuration
- 1/2 length, full profile, x8 edge PCIe form factor
- Four QSFP-DD cages for a total of 32 channels each capable of 28 Gpbs operation (total 896 Gbps)
- One 8-lane Ultraport SlimSAS connectors compliant with OpenCAPI and suitable for IO expansion
- Supports VU5P, VU9P Virtex UltraScale+ FPGAs in the A2104 package.
- Front panel and rear edge JTAG access via USB port
- FPGA configurable over USB/JTAG and SPI configuration flash
- Voltage, current, and temperature monitoring
- 8 GPIO signals and 1 isolated timing input
- User LEDs and timing input options.

1.2 Order Code

See http://www.alpha-data.com/pdfs/adm-pcie-9v5.pdf for complete ordering options.

2 Board Information

2.1 Physical Specifications

The ADM-PCIE-9V5 complies with PCI Express CEM revision 3.0.

Description	Measure
PCB Dy	100.15 mm
Total Dx	181.5 mm
PCB Dz	1.6 mm

Table 1 : Mechanical Dimensions (PCB only)

Description	Measure
Total Dy	120.9 mm
Total Dx	181.5 mm
Total Dz	19.7 mm
Weight	590 grams (without fan)

Table 2 : Mechanical Dimensions (Fully Assembled)

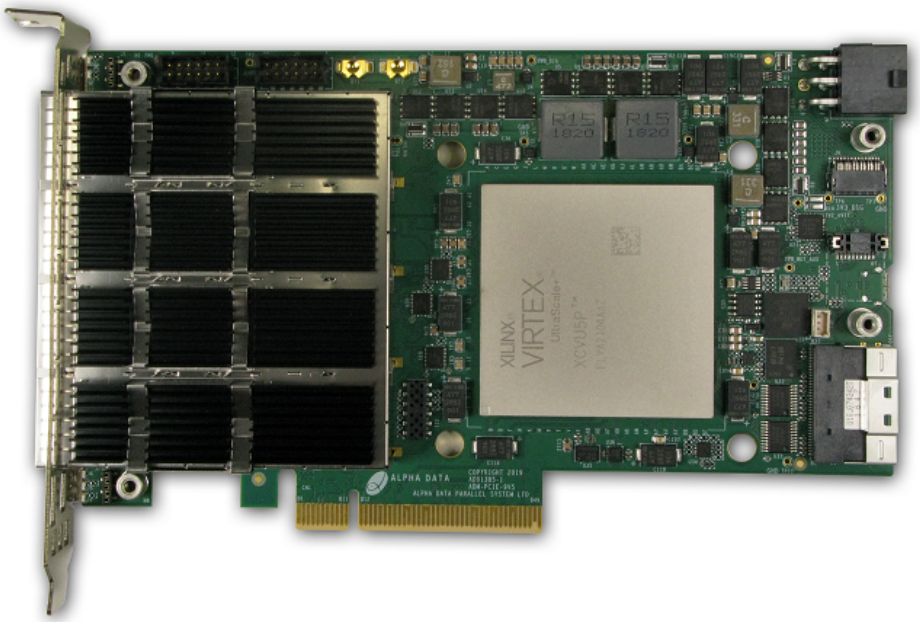

Figure 2 : ADM-PCIE-9V5 Top View

2.2 Chassis Requirements

2.2.1 PCI Express

The ADM-PCIE-9V5 is capable of PCIe Gen 3 with 8 lanes, using the Xilinx Integrated Block for PCI Express.

2.2.2 Mechanical Requirements

An 8 or 16 lane physical PCIe slot is required for mechanical compatibility.

2.2.3 Power Requirements

The ADM-PCIE-9V5 draws power from the PCIe Edge and the 6-pin ATX power connector. The ADM-PCIE-9V5 does not use or require the 3.3V power from the PCIe Edge (though it does use 3.3V AUX). Revision 1 cards (serial number less than 110) require both PCIe edge and 6-pin ATX power connector. Revision 2 and onward can operate with only the PCIe edge. To operate with PCIe edge only, ensure SW1-3 is OFF (see Switches). As per PCIe specification, users should limit the board power consumption to 66W when using only the PCIe edge power. Adding the 6-pin ATX connector provides additional 75W of power, bringing the total board power dissipation maximum to 141W.

Power consumption estimation requires the use of the Xilinx XPE spreadsheet and a power estimator tool available from Alpha Data. Please contact **support@alpha-data.com** to obtain this tool.

The power available to the rails calculated using XPE are as follows:

Voltage	Source Name	Current Capability
0.85-0.90	VCC_INT + VCCINT_IO + VCC_BRAM	80A
0.9	MGTAVCC	8A
1.2	MGTAVTT	15A
1.8	VCCAUX + VCCAUX_IO + VCCO_1.8V	3A
1.8	MGTVCCAUX	1A
3.3	3.3V for Optics	9A

Table 3 : Available Power By Rail

2.2.4 KN32 – Emissions

Type of Equipment	User's Guide
A급 기기 (업무용 방송통신기자재)	이 기기는 업무용(A급) 전자파적합기기로서 판매자 또는 사용자는 이 점을 주의하시기 바라며, 가정외의 지역에서 사용하는 것을 목적으로 합니다.
Class A Equipment (Industrial Broadcasting & Communication Equipment)	This equipment is **Industrial (Class A) electromagnetic wave suitability equipment** and seller or user should take notice of it, and this equipment is to be used in the places except for home.

Figure 3 : KN32 – Emissions

2.3 Thermal Performance

If the FPGA core temperature exceeds 105 degrees Celsius, the FPGA design will be cleared to prevent the card from over-heating.

The ADM-PCIE-9V5 comes with a heat sink to help avoid thermal overstress of FPGA, since it is typically the hottest point on the card. The FPGA die temperature must remain under 100 degrees Celsius. To calculate the FPGA die temperature, take your application power, multiply by Theta JA from the table below, and add to your system internal ambient temperature. If you are using the fan provided with the board, you will find theta JA is approximately 0.88 degC/W for the board in still air.

The power dissipation can be estimated by using the Alpha Data power estimator in conjunction with the Xilinx Power Estimator (XPE) downloadable at http://www.xilinx.com/products/technology/power/xpe.html. Download the UltraScale tool and set the device according to your part number details: Virtex UltraScale+, VU13P/VU9P, A2104 package, -2/-3 speed grade, extended. Set the ambient temperature to your system ambient and select 'user override' for the effective theta JA and enter the figure associated with your system LFM in the blank field. Proceed to enter all applicable design elements and utilization in the following spreadsheet tabs. Next acquire the 9V5 power estimator from Alpha Data by contacting support@alpha-data.com. You will then plug in the FPGA power figures along with Optical module figures to get a board level estimate.

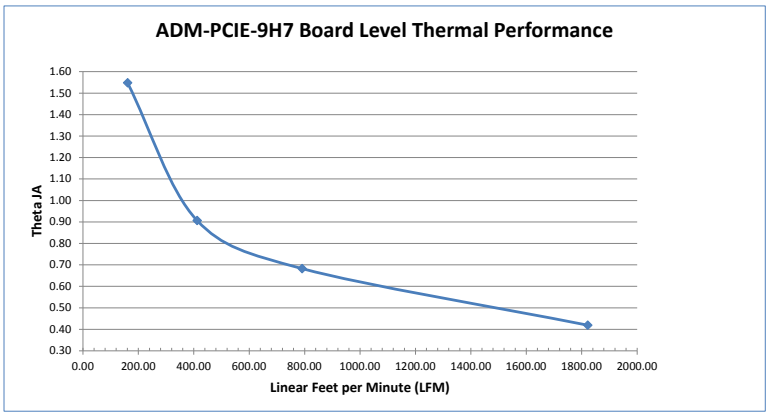

Figure 4 : Thermal Performance

2.3.1 Active VS Passive Thermal Management

The ADM-PCIE-9V5 ships with a small optional blower for active cooling in systems with poor airflow. If the ADM-PCIE-9V5 will be installed in a server with controlled airflow, the card may be ordered without the additional fan hardware. The fans have a much shorter mean time between failure (MTBF) than the rest of the assembly, so passive cards have much longer life expectance before requiring maintenance. The ADM-PCIE-9V5 also includes a fan speed controller, allowing variable fan speed based on die temperature, and detection of a failed fan (see section Fan Controllers).

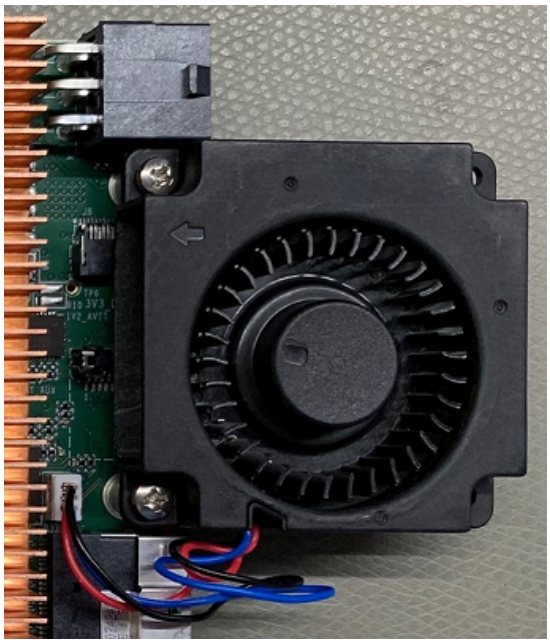

Figure 5 : ADM-PCIE-9V5 Fan

2.4 Customizations

Alpha Data provides extensive customization options to existing commercial off-the-shelf (COTS) products. Some options include, but are not limited to: additional networking cages in adjacent slots, enhanced heat sinks, baffles, and circuit additions.

Please contact sales@alpha-data.com to get a quote and start your project today.

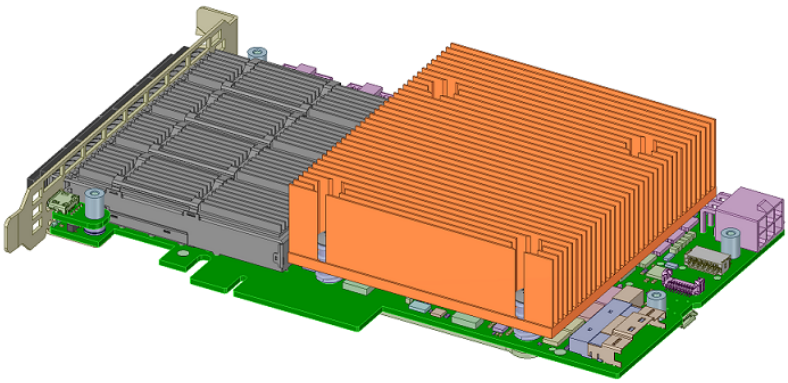

Figure 6 : ADM-PCIE-9V5 2-slot enhanced heat sink

3 Functional Description

3.1 Overview

The ADM-PCIE-9V5 is a versatile reconfigurable computing platform with a Virtex UltraScale+ VU5P/VU9P FPGA, a Gen3x8 PCIe interface, four QSFP-DD cages, an OpenCAPI compatible Ultraport SlimSAS connector also capable of 28G/channel, an isolated input for a timing synchronization pulse, a 12 pin header for general purpose use (clocking, control pins, debug, etc.), front panel LEDs, and a robust system monitor.

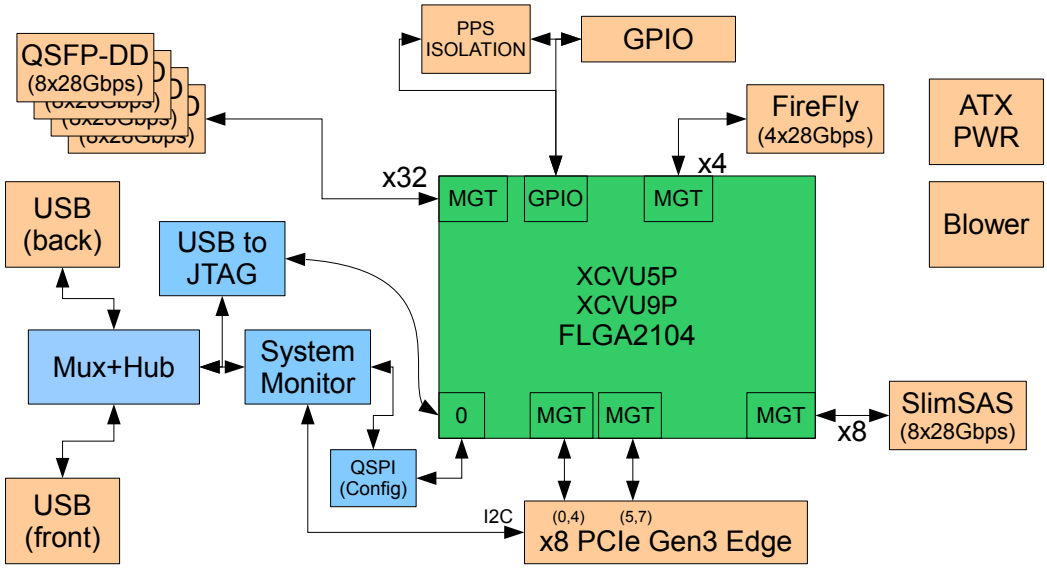

Figure 7 : ADM-PCIE-9V5 Block Diagram

3.1.1 Switches

The ADM-PCIE-9V5 has an octal DIP switch SW1, located on the rear side of the board. The function of each switch in SW1 is detailed below:

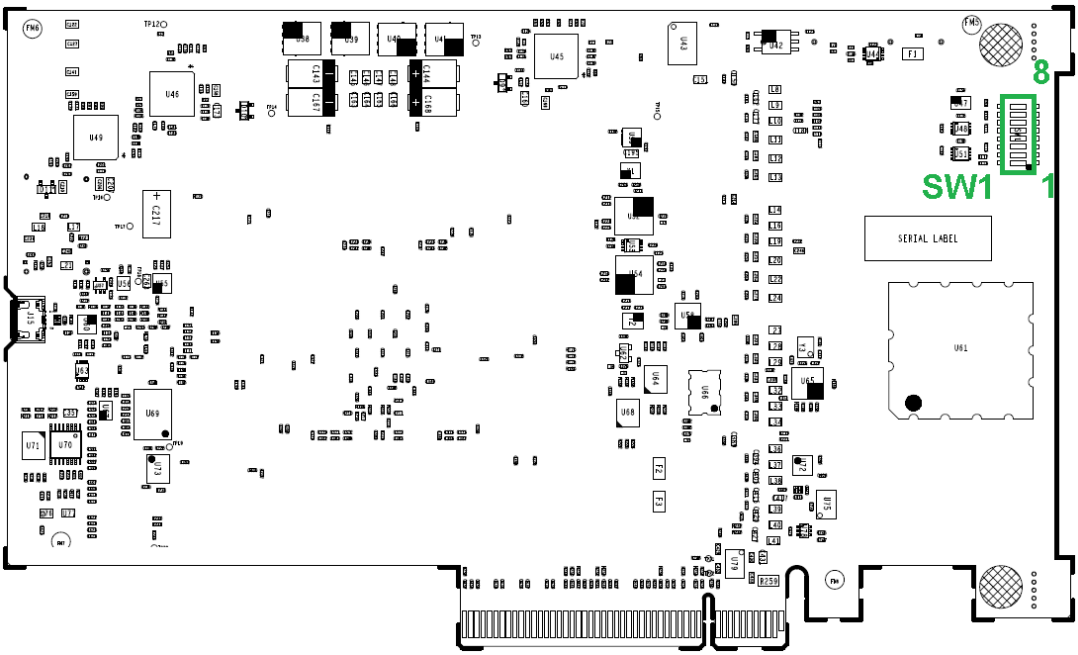

Figure 8 : Switches

Switch	Factory Default	Function	OFF State	ON State
SW1-1	OFF	User Switch 0	Pin AW33 = '1'	Pin BF52 = '0'
SW1-2	OFF	User Switch 1	Pin AY36 = '1'	Pin BF47 = '0'
SW1-3	ON	12V Auto-detect	12V PCIe edge auto-detect	ATX AUX power required
SW1-4	OFF	Power Off	Board will power up	Immediately power down
SW1-5	OFF	Service Mode	System Monitor normal operation	System Monitor Service Mode (firmware update etc.)
SW1-6	ON	HOST_I2C_EN	System Monitor connected to PCIe slot I2C	System Monitor isolated from PCIe slot I2C
SW1-7	ON	CAPI_VPD_EN	OpenCAPI VPD PROM connected to PCIe slot I2C	OpenCAPI VPD PROM isolated from PCIe slot I2C
SW1-8	ON	OpenCAPI_VPD_WP	OpenCAPI VPD is write protected	CAPI VPD is writable

Table 4 : Switch Functions

Use I/O Standard "LVCMOS18" when constraining the User Switch pins.

3.1.2 LEDs

There are 9 LEDs on the ADM-PCIE-9V5, 6 of which are general purpose and whose meaning can be defined by the user. The other 3 have fixed functions described below:

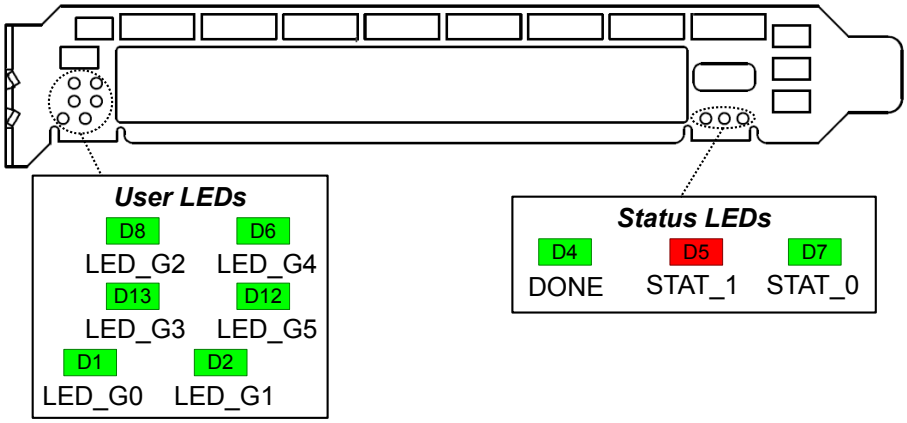

Figure 9 : Front Panel LEDs

Comp. Ref.	Function	ON State	OFF State
D1	USER_LED_G0_1V8	User defined '0'	User defined '1'
D2	USER_LED_G1_1V8	User defined '0'	User defined '1'
D8	USER_LED_G2_1V8	User defined '0'	User defined '1'
D13	USER_LED_G3_1V8	User defined '0'	User defined '1'
D6	USER_LED_G4_1V8	User defined '0'	User defined '1'
D12	USER_LED_G5_1V8	User defined '0'	User defined '1'
D4	DONE	FPGA is configured	FPGA is not configured
D5	Status 1	See Status LED Definitions	
D7	Status 0	See Status LED Definitions	

Table 5 : LED Details

See Section Complete Pinout Table for full list of user controlled LED nets and pins

3.2 Clocking

The ADM-PCIE-9V5 provides flexible reference clock solutions for the many multi-gigabit transceiver quads and FPGA fabric. Any programmable clock, from the SI5338 Clock Synthesizer, is re-configurable from the front panel USB Interface by using Alpha Data's avr2util utility. This allows the user to configure almost any arbitrary clock frequency during application run time. The maximum clock frequency is 312.5MHz. Customers who purchase RD-9V5 also have the option of embedding IP into their FPGA design that permits programmable clock re-configuration via PCIe or from within the FPGA.

There is also two available Si5328 jitter attenuator. These can provide clean and synchronous clocks to the QSFP-DD and OpenCAPI (SlimSAS) quad locations at many clock frequencies. These devices only use volatile memory, so the FPGA design will need to re-configure the register map after any power cycle event.

All clock names in the section below can be found in Complete Pinout Table.

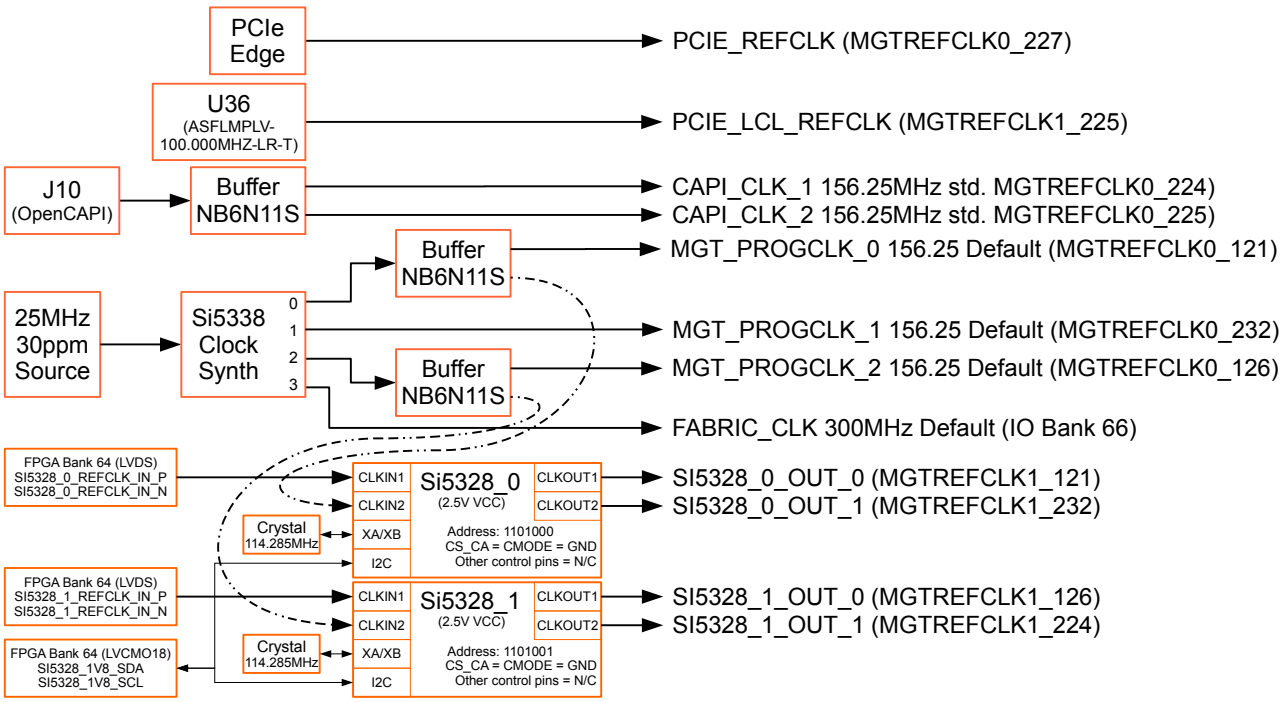

Figure 10 : Clock Topology

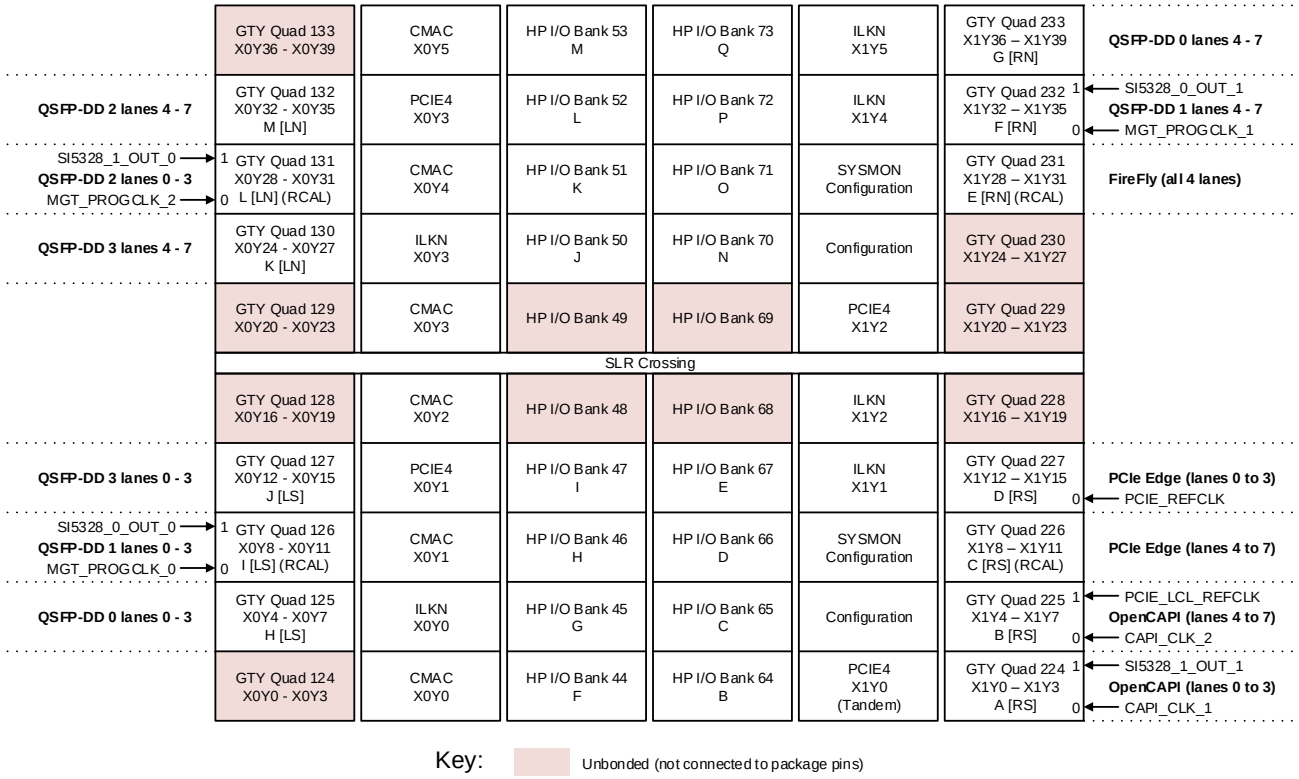

Figure 11 : VU5P FPGA Clock Location

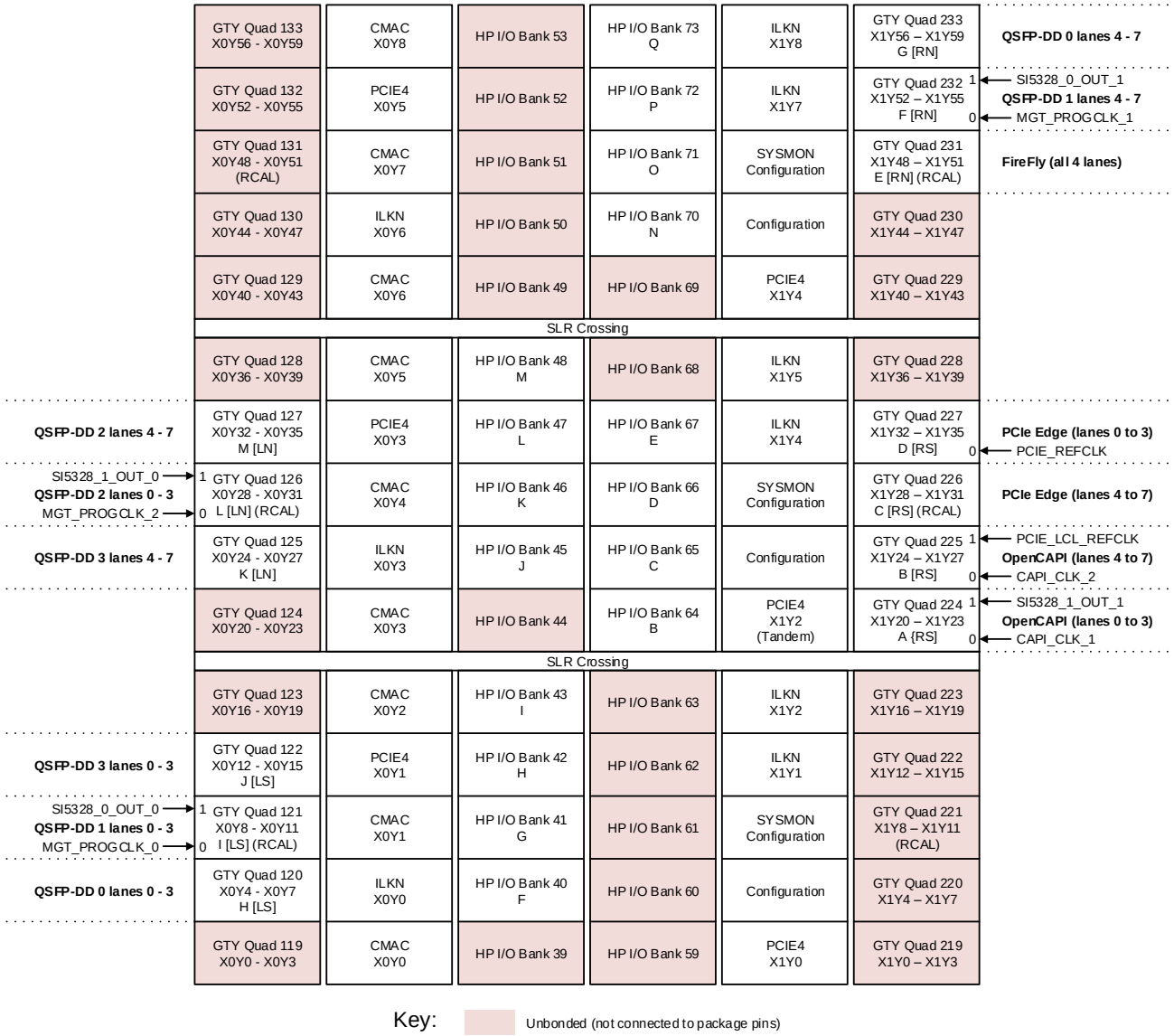

Figure 12 : VU9P FPGA Clock Location

3.2.1 Si5328

If jitter attenuation is required please see the reference documentation for the Si5328.
https://www.silabs.com/Support%20Documents/TechnicalDocs/Si5328.pdf

The circuit connections mirror the Xilinx VCU108 Development Kits (page 57 of the schematic, component U57). The MGT RXOUTCLK can be used to pass a recovered clock to the FPGA fabric. Please refer to Xilinx UG578 and the VCU108 for more information.

The CLKIN2 input of the SI5328, provided by the SI5338, is only available in rev2 PCBs and onward (Serial number greater than 109).

3.2.2 PCIe Reference Clocks

The 8 MGT lanes connected to the PCIe card edge use MGT tiles 226 through 227 and use the system 100 MHz clock (net name PCIE_REFCLK).

Alternatively, a clean, onboard 100MHz clock is available as well (net name PCIE_LCL_REFCLK).

3.2.3 Fabric Clock

The design offers a fabric clock (net name FABRIC_CLK_*) which defaults to 300 MHz. This clock is intended to be used for IDELAY elements in FPGA designs. The fabric clock is connected to a Global Clock (GC) pin.

DIFF_TERM_ADV = TERM_100 is required for LVDS termination

3.2.4 Programming Clock (EMCCLK)

A 100MHz clock (net name EMCCLK_B) is fed into the EMCCLK pin to drive the SPI flash device during configuration of the FPGA. Note that this is not a global clock capable IO pin.

3.2.5 QSFP-DD Clock

The QSFP-DD clocks have a default 156.25MHz reference clock. Note that this clock frequency can be changed to any arbitrary clock frequency up to 312MHz by re-programing the Si5338 reprogrammable clock oscillator. See details on avr2util in the section: USB Interface.

See net names MGT_PROGCLK_* for pin locations.

The QSFP-DD cages are also located such that they can be clocked from the Si5328 jitter attenuators.

See net names SI5328_OUT_* for pin locations.

3.2.6 Ultraport SlimSAS (OpenCAPI)

The Ultraport SlimSAS connector is located in MGT tile 224 and 225.

For OpenCAPI an external 156.25MHz clock is provided over the cable. See net names CAPI_CLK_* for cable clock pin locations.

Another alternative clock source for this interface is the PCIE_LCL_REFCLK clock synthesizer at 100MHz.

For jitter sensitive applications, this interface can be clocked from the Si5328 jitter attenuator. See net names SI5328_OUT_* for pin locations.

3.3 PCI Express

The ADM-PCIE-9V5 is capable of PCIe Gen 3 with 8 lanes. The FPGA drives these lanes directly using the Integrated PCI Express block from Xilinx. Negotiation of PCIe link speed and number of lanes used is generally automatic and does not require user intervention.

PCI Express reset (PERST#) connected to the FPGA through a buffer. See Complete Pinout Table signal PERST0_1V8_L.

The other pin assignments for the high speed lanes are provided in the pinout attached to the Complete Pinout Table

The PCI Express specification requires that all add-in cards be ready for enumeration within 120ms after power is valid (100ms after power is valid + 20ms after PERST is released). The ADM-PCIE-9V5 does meet this requirement when configured from a tandem bitstream with the proper SPI constraints detailed in the section: Configuration From Flash Memory. For more details on tandem configuration, see Xilinx xapp 1179.

Note:
Different motherboards/backplanes will benefit from different RX equalization schemes within the PCIe IP core provided by Xilinx. Alpha Data recommends using the following setting if a user experiences link errors or training issues with their system: within the IP core generator, change the mode to "Advanced" and open the "GT Settings" tab, change the "form factor driven insertion loss adjustment" from "Add-in Card" to "Chip-to-Chip" (See Xilinx PG195, PG213, and PG239 for more details).

3.4 QSFP-DD

Four QSFP-DD cages are available at the front panel. These cages are capable of housing either QSFP28 or QSFP-DD cables (backwards compatible). Both active optical and passive copper QSFP-DD/QSFP28 compatible models are fully compliant. The communication interface can run at up to 28Gbps per channel. Each QSFP-DD cage has 8 channels (total maximum bandwidth of 224Gbps per cage). This cage is ideally suited for 8x 10G/25G, 2x 100G Ethernet, or any other protocol supported by the Xilinx GTY Transceivers. Please see Xilinx User Guide UG578 for more details on the capabilities of the transceivers.

All QSFP-DD cages have control signals connected to the FPGA. Their connectivity is detailed in the Complete Pinout Table at the end of this document. The notation used in the pin assignments is QSFP_0*, QSFP_1*, QSFP_2*, and QSFP_3*, with locations clarified in the diagram below.

The Management Interface of each QSFP-DD cage is connected to the FPGA, as detailed in Complete Pinout Table. The available signals are SDA/SCL (I2C), INT_L (interrupt), LPMODE (low power mode), RST_L (reset), and MODPRS_L (module present).

Note:
The LPMODE (Low Power Mode) to the cage is pulled up by default. The FPGA can either (a) drive the relevant LPMODE pin low or (b) issue I2C transactions in order to power-up a given QSFP-DD/QSFP28 module

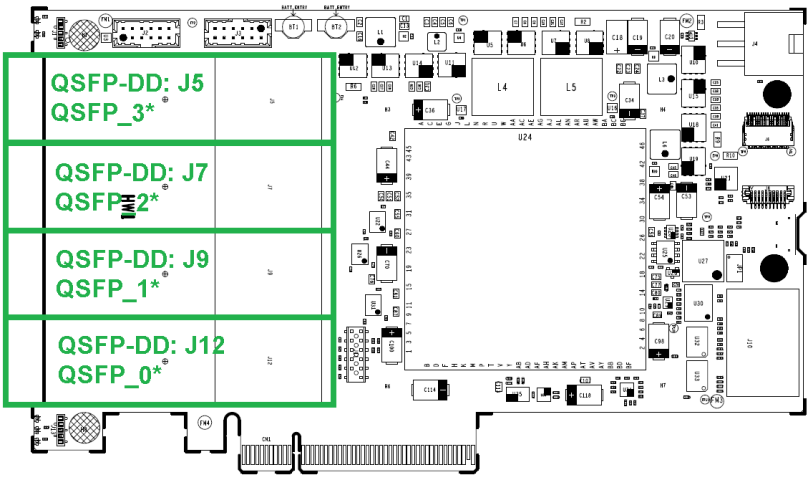

Figure 13 : QSFP-DD Location

It is possible for Alpha Data to pre-fit the ADM-PCIE-9V5 with QSFP-DD and QSFP28 components. Please contact sales@alpha-data.com for full details and options.

Alpha Data has tested the ADM-PCIE-9V5 with an array of passive cables from multiple manufacturers. Please contact sales@alpha-data.com for more details on appropriate and available cables. Cable types include: QSFP-DD to 8x SFP, QSFP-DD to 2x QSFP, and QSFP-DD to QSFP-DD.

3.5 OpenCAPI Ultraport SlimSAS

An Ultraport SlimSAS receptacle along the back of the board allows for OpenCAPI compliant interfaces running at 200G (8 channels at 25G). Please contact support@alpha-data.com or your IBM representative for more details on OpenCAPI and its benefits.

The SlimSAS connector can also be used to connect multiple ADM-PCIE-9V5 cards within a chassis.

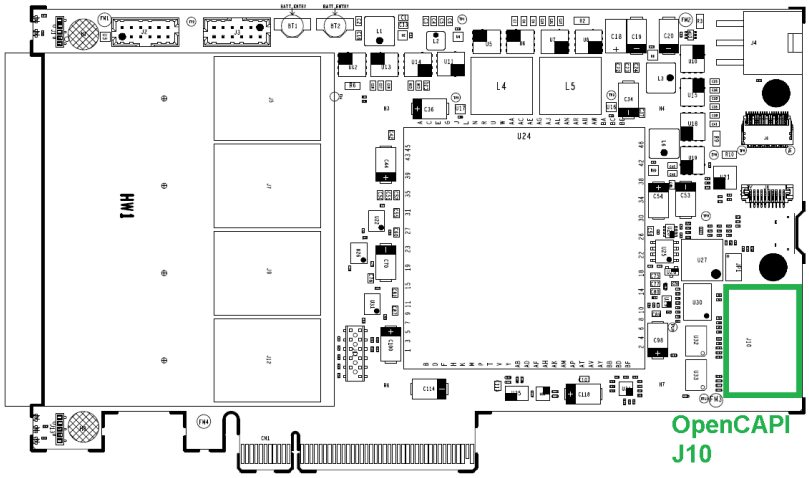

Figure 14 : OpenCAPI Location

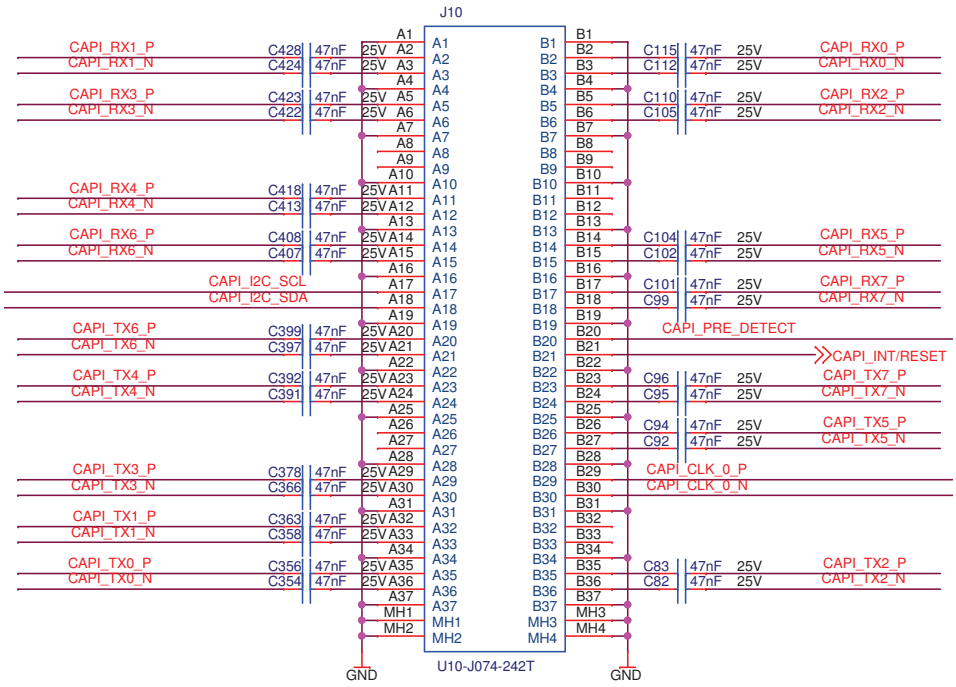

Figure 15 : OpenCAPI Pinout

3.6 System Monitor

The ADM-PCIE-9V5 has the ability to monitor its own temperature and the voltages and currents of certain power supply rails, in order to provide an indication of board health. The monitoring is implemented using an Atmel AVR microcontroller.

If the core FPGA temperature exceeds 105 degrees Celsius, the FPGA will be cleared to prevent damage to the card.

The microcontroller monitors power supply rail voltages & currents and temperatures at certain points on the board. This information can be read out via USB using the avr2util utility, and also via PCIe if RD-9V5 is purchased.

Monitors	Identifier	Purpose/Description
ETC	ETC	Elapsed time counter (seconds)
EC	EC	Event counter (power cycles)
12V_AUX	ADC00	12v board input supply from 6-pin ATX Cable
12V_AUX_I	ADC01	12V input current from 6-pin ATX Cable in amps
12V_EDGE	ADC02	12V board input supply from PCIe Edge
12V_EDGE_I	ADC03	12V board input current from PCIe Edge in amps
3V3_EDGE	ADC04	3.3V board input supply from PCIe edge (unused)
3V3_AUX	ADC05	3.3V auxilary board input supply from PCIE edge
3V3_DIG	ADC06	3.3V generated onboard for QSFP optics
2V5_CLK	ADC07	2.5V generated onboard for clock circuitry
1V8_DIG	ADC08	1.8V generated onboard fpr FPGA IO voltage (VCCO)
1V8_MGT_AUX	ADC09	1.8V generated onboard for transceiver power (AVCC_AUX)
1V2_AVTT	ADC10	1.2V generated onboard for transceiver Power (AVTT)
0V9_AVCC	ADC11	0.9V generated onboard for transceiver Power (AVCC)
VCC_INT	ADC12	0.85-0.90V generated onboard for VccINT + VccBRAM + VccINT_IO
GND	ADC13	0V electrical ground
uC_Temp	TMP00	uC on-die temperature
Board0_Temp	TMP01	Board temperature near front panel (U3)
Board1_Temp	TMP02	Board temperature near back edge (U23)
FPGA_Temp	TMP03	FPGA on-die temperature

Table 6 : Voltage, Current, and Temperature Monitors

3.6.1 System Monitor Status LEDs

LEDs D5 (Red) and D7 (Green) indicate the card health status.

LEDs	*Status*
Green	Running and no alarms
Green + Red	Standby (Powered off)
Flashing Green + Flashing Red (together)	Attention - critical alarm active
Flashing Green + Flashing Red (alternating)	Service Mode
Flashing Green + Red	Attention - alarm active
Red	Missing application firmware or invalid firmware
Flashing Red	FPGA configuration cleared to protect board

Table 7 : Status LED Definitions

3.6.2 Fan Controllers

The onboard USB bus controlled by the system monitor has access to a MAX6620 fan controller. This device can be controlled through the multiple onboard system monitor communication interfaces, including USB, PCIe Edge SMBUS, and FPGA sysmon seral communication port. The fan controller is on I2C bus 1 at address 0x2a. For additional questions. Contact support@alpha-data.com with additional questions on utilizing these controllers.

3.7 USB Interface

The FPGA can be configured directly from the USB connection on either the front panel or the rear card edge. The ADM-PCIE-9V5 utilizes the Digilent USB-JTAG converter box which is supported by the Xilinx software tool suite. Simply connect a micro-USB AB type cable between the ADM-PCIE-9V5 USB port and a host computer with Vivado installed. Vivado Hardware Manager will automatically recognize the FPGA and allow you to configure the FPGA and the SPI configuration Flash memory.

The same USB connector is used to directly access the system monitor system. All voltages, currents, temperatures, and non-volatile clock configuration settings can be accessed using Alpha Data's avr2util software at this interface.

Avr2util for Windows and the associated USB driver is downloadable here:
https://support.alpha-data.com/pub/firmware/utilities/windows/

Avr2util for Linux is downloadable here:
https://support.alpha-data.com/pub/firmware/utilities/linux/

Use "avr2util.exe /?" to see all options.

For example "avr2util.exe /usbcom com4 display-sensors" will display all sensor values.

For example "avr2util.exe /usbcom com4 setclknv 1 100000000" will set the MGT_PROGCLK_1 100MHz. setclk index 0 = MGT_PROGCLK_1, index 1 = MGT_PROGCLK_1, index 2 = MGT_PROGCLK_2, index 3 = FABRIC_CLK.

Change 'com4' to match the com port number assigned under windows device manager.

3.8 Configuration

There are two main ways of configuring the FPGA on the ADM-PCIE-9V5:

- From Flash memory, at power-on, as described in Section 3.8.1
- Using USB cable connected at either USB port Section 3.8.2

3.8.1 Configuration From Flash Memory

The FPGA can be automatically configured at power-on from two 1 Gbit QSPI flash memory device configured as an x8 SPI device (Micron part numbers MT25QU01GBBB8E12-0). These flash devices are typically divided into two regions of 128 MiByte each, where each region is sufficiently large to hold an uncompressed bitstream for a VU5P or VU9P FPGA.

The ADM-PCIE-9V5 is shipped with a simple PCIe endpoint bitstream which should be visible to the operating system (using e.g. Windows Device Manager or “lspci” in Linux) in order to provided confidence that the card is working correctly when installed in a system. On request, Alpha Data can pre-load custom bitstreams during production test. Please contact sales@alpha-data.com in order to discuss this possibility.

It is possible to use Multiboot with a fallback image on this hardware. The master SPI configuration interface and the Fallback MultiBoot are discussed in detail in Xilinx UG570.

At power-on, the FPGA attempts to configure itself automatically in SPI master mode, depending on the header of the bitstream that has been flashed into the card. This normally results in SPIx8 configuration at EMCCLK frequency. The configuration scheme used in the ADM-PCIE-9V5 is compatible with Multiboot; see Xilinx UG570 for details. The FPGA can also be made to reconfigure itself from an arbitrary Flash address using the ICAPE3 primitive; this is also described in Xilinx UG570.

The image loaded can also support tandem PROM or tandem PCIE with field update configuration methods. These options reduce power-on load times to help meet the PCIe reset timing requirements. Tandem with field also enables a host system to reconfigure the user FPGA logic without losing the PCIe link, a useful feature when system resets and power cycles are not an option.

The Alpha Data System Monitor is also capable of reconfiguring the flash memory and reprograming the FPGA. This provides a useful failsafe mechanism to re-program the FPGA even if it drops off the PCIe bus. The system monitor can be accessed with avr2util over USB at the front panel and rear edge.

3.8.1.1 Building and Programming Configuration Images

Generate a bitfile with these constraints (see xapp1233):

- set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
- set_property BITSTREAM.CONFIG.EXTMASTERCCLK_EN {DIV-1} [current_design]
- set_property BITSTREAM.CONFIG.SPI_32BIT_ADDR YES [current_design]
- set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 8 [current_design]
- set_property BITSTREAM.CONFIG.SPI_FALL_EDGE YES [current_design]
- set_property BITSTREAM.CONFIG.UNUSEDPIN {Pullnone} [current_design]
- set_property CFGBVS GND [current_design]
- set_property CONFIG_VOLTAGE 1.8 [current_design]
- set_property BITSTREAM.CONFIG.OVERTEMPSHUTDOWN Enable [current_design]

Generate an MCS file with these properties (write_cfgmem):

- -format MCS
- -size 256
- -interface SPIx8
- -loadbit "up 0x0000000 <directory/to/file/filename.bit>" (0th location)

Program with vivado hardware manager with these settings (see xapp1233):

- SPI part: mt25qu01g-spi-x1_x2_x4_x8
- State of non-config mem I/O pins: Pull-none

3.8.2 Configuration via JTAG

A micro-USB AB Cable may be attached to the front panel or rear edge USB port. This permits the FPGA to be reconfigured using the Xilinx Vivado Hardware Manager via the integrated Digilent JTAG converter box. The device will be automatically recognized in Vivado Hardware Manager.

For more detailed instructions, please see “Using a Vivado Hardware Manager to Program an FPGA Device” section of Xilinx UG908: https://www.xilinx.com/support/documentation/sw_manuals/xilinx2014_1/ug908-vivado-programming-debugging.pdf

3.9 GPIO Connector

The GPIO option consists of a versatile shrouded connector from Molex with part number 87832-1222. This connector gives users eight signals connected to the FPGA.

Recommended mating plug: Molex 0875681273 or 0511101260

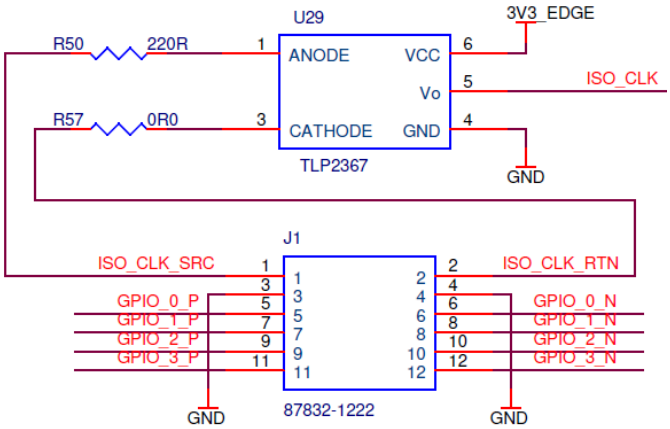

Figure 16 : GPIO Connector Schematic

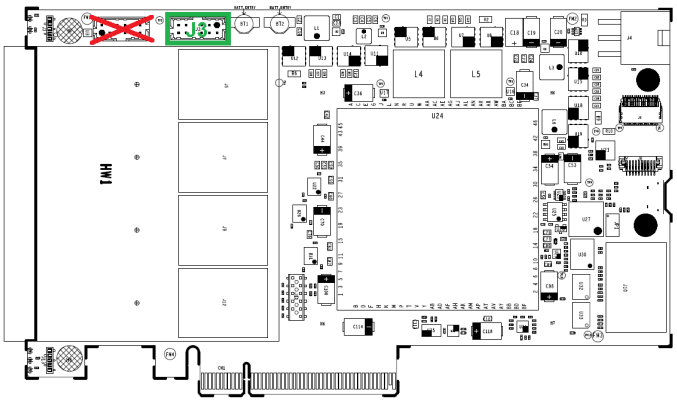

Figure 17 : GPIO Connector Location

3.9.1 Direct Connect FPGA Signals

8 nets are broken out to the GPIO header, as four sets of differential pairs. These signal are suitable for any 1.8V signalling standards supported by the Xilinx UltraScale architecture. See Xilinx UG571 for IO options. LVDS and 1.8 CMOS are popular options. The 0th GPIO signal index is suitable for a global clock connection.

The direct connect GPIO signals are limited to 1.8V by a quickswitch (74CBTLVD3245PW) in order to protect the FPGA from overvoltage on IO pins. This quickswitch allows the signals to travel in either direction with only 4 ohms of series impedance and less than 1ns of propagation delay. The nets are directly connected to the FPGA after the quickswitch.

Direct connect signal names are labeled GPIO_0_1V8_P/N and GPIO_1_1V8_P/N, etc. to show polarity and grouping. The signal pin allocations can be found in Complete Pinout Table

3.9.2 Timing Input

Pins 1 and 2 of J1 can be used as an isolated timing input signal (up to 25MHz). Applications can either directly connect to the GPIO connector, or Alpha Data can provide a cabled solution with an SMA or similar connector on the front panel. Contact sales@alpha-data.com for front panel connector options.

For pin locations, see signal name ISO_CLK in Complete Pinout Table.

The signal is isolated through a optical isolator part number TLP2367 with 220 ohm of series resistance.

3.10 User EEPROM

A 2Kb I2C user EEPROM is provided for storing MAC addresses or other user information. The EEPROM is part number CAT34C02HU4IGT4A

The address pins A2, A1, and A0 are all strapped to a logical '0'.

Write protect (WP), Serial Clock (SCL), and Serial Data (SDA) pin assignments can be found in Complete Pinout Table with the names SPARE_WP, SPARE_SCL, and SPARE_SDA respectively.

WP, SDA, and SCL signals all have external pull-up resistors on the card.

Appendix A: Complete Pinout Table

Pin Number	Signal Name	Pin Name	Bank Voltage
BF12	AVR_B2U_1V8	IO_L2P_T0L_N2_66	1.8 (LVCMOS18)
BD12	AVR_HS_B2U_1V8	IO_L1P_T0L_N0_DBC_66	1.8 (LVCMOS18)
BC8	AVR_HS_CLK_1V8	IO_L12N_T1U_N11_GC_66	1.8 (LVCMOS18)
BE12	AVR_HS_U2B_1V8	IO_L1N_T0L_N1_DBC_66	1.8 (LVCMOS18)
BC9	AVR_MON_CLK_1V8	IO_L12P_T1U_N10_GC_66	1.8 (LVCMOS18)
BF11	AVR_U2B_1V8	IO_L2N_T0L_N3_66	1.8 (LVCMOS18)
AR8	CAPI_CLK_1_PIN_N	MGTREFCLK0N_224	MGT REFCLK
AR9	CAPI_CLK_1_PIN_P	MGTREFCLK0P_224	MGT REFCLK
AL8	CAPI_CLK_2_PIN_N	MGTREFCLK0N_225	MGT REFCLK
AL9	CAPI_CLK_2_PIN_P	MGTREFCLK0P_225	MGT REFCLK
BE24	CAPI_I2C_SCL_1V8	IO_L1P_T0L_N0_DBC_64	1.8 (LVCMOS18)
BF24	CAPI_I2C_SDA_1V8	IO_L1N_T0L_N1_DBC_64	1.8 (LVCMOS18)
BC23	CAPI_INT/RESET_1V8	IO_L2P_T0L_N2_64	1.8 (LVCMOS18)
BB1	CAPI_RX0_N	MGTYRXN0_224	MGT
BB2	CAPI_RX0_P	MGTYRXP0_224	MGT
AY1	CAPI_RX1_N	MGTYRXN1_224	MGT
AY2	CAPI_RX1_P	MGTYRXP1_224	MGT
AV1	CAPI_RX2_N	MGTYRXN2_224	MGT
AV2	CAPI_RX2_P	MGTYRXP2_224	MGT
AT1	CAPI_RX3_N	MGTYRXN3_224	MGT
AT2	CAPI_RX3_P	MGTYRXP3_224	MGT
AP1	CAPI_RX4_N	MGTYRXN0_225	MGT
AP2	CAPI_RX4_P	MGTYRXP0_225	MGT
AM1	CAPI_RX5_N	MGTYRXN1_225	MGT
AM2	CAPI_RX5_P	MGTYRXP1_225	MGT
AK1	CAPI_RX6_N	MGTYRXN2_225	MGT
AK2	CAPI_RX6_P	MGTYRXP2_225	MGT
AJ3	CAPI_RX7_N	MGTYRXN3_225	MGT
AJ4	CAPI_RX7_P	MGTYRXP3_225	MGT
BE4	CAPI_TX0_N	MGTYTXN0_224	MGT
BE5	CAPI_TX0_P	MGTYTXP0_224	MGT
BC4	CAPI_TX1_N	MGTYTXN1_224	MGT
BC5	CAPI_TX1_P	MGTYTXP1_224	MGT

Table 8 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	Bank Voltage
BA4	CAPI_TX2_N	MGTYTXN2_224	MGT
BA5	CAPI_TX2_P	MGTYTXP2_224	MGT
AW4	CAPI_TX3_N	MGTYTXN3_224	MGT
AW5	CAPI_TX3_P	MGTYTXP3_224	MGT
AU4	CAPI_TX4_N	MGTYTXN0_225	MGT
AU5	CAPI_TX4_P	MGTYTXP0_225	MGT
AT6	CAPI_TX5_N	MGTYTXN1_225	MGT
AT7	CAPI_TX5_P	MGTYTXP1_225	MGT
AR4	CAPI_TX6_N	MGTYTXN2_225	MGT
AR5	CAPI_TX6_P	MGTYTXP2_225	MGT
AP6	CAPI_TX7_N	MGTYTXN3_225	MGT
AP7	CAPI_TX7_P	MGTYTXP3_225	MGT
AF13	CCLK	CCLK_0	1.8 (LVCMOS18)
AE12	DONE_1V8	DONE_0	1.8 (LVCMOS18)
AL20	EMCCLK_B	IO_L24P_T3U_N10_EMCCLK_65	1.8 (LVCMOS18)
BA9	FABRIC_CLK_PIN_N	IO_L13N_T2L_N1_GC_QBC_66	1.8 (LVDS with DIFF_TERM_ADV)
AY9	FABRIC_CLK_PIN_P	IO_L13P_T2L_N0_GC_QBC_66	1.8 (LVDS with DIFF_TERM_ADV)
G22	FIREFLY_INT_1V8_L	IO_L13P_T2L_N0_GC_QBC_72	1.8 (LVCMOS18)
R21	FIREFLY_MODPRS_L	IO_L3P_T0L_N4_AD15P_72	1.8 (LVCMOS18)
G21	FIREFLY_RST_1V8_L	IO_L13N_T2L_N1_GC_QBC_72	1.8 (LVCMOS18)
Y1	FIREFLY_RX0_N	MGTYRXN0_231	MGT
Y2	FIREFLY_RX0_P	MGTYRXP0_231	MGT
W3	FIREFLY_RX1_N	MGTYRXN1_231	MGT
W4	FIREFLY_RX1_P	MGTYRXP1_231	MGT
V1	FIREFLY_RX2_N	MGTYRXN2_231	MGT
V2	FIREFLY_RX2_P	MGTYRXP2_231	MGT
U3	FIREFLY_RX3_N	MGTYRXN3_231	MGT
U4	FIREFLY_RX3_P	MGTYRXP3_231	MGT
H22	FIREFLY_SCL_1V8	IO_L14N_T2L_N3_GC_72	1.8 (LVCMOS18)
H23	FIREFLY_SDA_1V8	IO_L14P_T2L_N2_GC_72	1.8 (LVCMOS18)
V6	FIREFLY_TX0_N	MGTYTXN0_231	MGT
V7	FIREFLY_TX0_P	MGTYTXP0_231	MGT
T6	FIREFLY_TX1_N	MGTYTXN1_231	MGT
T7	FIREFLY_TX1_P	MGTYTXP1_231	MGT

Table 8 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	Bank Voltage
P6	FIREFLY_TX2_N	MGTYTXN2_231	MGT
P7	FIREFLY_TX2_P	MGTYTXP2_231	MGT
M6	FIREFLY_TX3_N	MGTYTXN3_231	MGT
M7	FIREFLY_TX3_P	MGTYTXP3_231	MGT
AJ11	FPGA_FLASH_CE0_L	RDWR_FCS_B_0	1.8 (LVCMOS18)
BF16	FPGA_FLASH_CE1_L	IO_L2N_T0L_N3_FWE_FCS2_B_65	1.8 (LVCMOS18)
AP11	FPGA_FLASH_DQ0	D00_MOSI_0	1.8 (LVCMOS18)
AN11	FPGA_FLASH_DQ1	D01_DIN_0	1.8 (LVCMOS18)
AM11	FPGA_FLASH_DQ2	D02_0	1.8 (LVCMOS18)
AL11	FPGA_FLASH_DQ3	D03_0	1.8 (LVCMOS18)
AM19	FPGA_FLASH_DQ4	IO_L22P_T3U_N6_DBC_AD0P-_D04_65	1.8 (LVCMOS18)
AM18	FPGA_FLASH_DQ5	IO_L22N_T3U_N7_DBC_AD0N-_D05_65	1.8 (LVCMOS18)
AN20	FPGA_FLASH_DQ6	IO_L21P_T3L_N4_AD8P_D06_65	1.8 (LVCMOS18)
AP20	FPGA_FLASH_DQ7	IO_L21N_T3L_N5_AD8N_D07_65	1.8 (LVCMOS18)
AV23	GPIO_0_1V8_N	IO_L14N_T2L_N3_GC_64	1.8 (LVCMOS18or LVDS)
AU23	GPIO_0_1V8_P	IO_L14P_T2L_N2_GC_64	1.8 (LVCMOS18or LVDS)
AV21	GPIO_1_1V8_N	IO_L15N_T2L_N5_AD11N_64	1.8 (LVCMOS18or LVDS)
AU21	GPIO_1_1V8_P	IO_L15P_T2L_N4_AD11P_64	1.8 (LVCMOS18or LVDS)
AV24	GPIO_2_1V8_N	IO_L16N_T2U_N7_QBC_AD3N_64	1.8 (LVCMOS18or LVDS)
AU24	GPIO_2_1V8_P	IO_L16P_T2U_N6_QBC_AD3P_64	1.8 (LVCMOS18or LVDS)
AR22	GPIO_3_1V8_N	IO_L17N_T2U_N9_AD10N_64	1.8 (LVCMOS18or LVDS)
AR23	GPIO_3_1V8_P	IO_L17P_T2U_N8_AD10P_64	1.8 (LVCMOS18or LVDS)
AC12	INIT_B_1V8	INIT_B_0	1.8 (LVCMOS18)
AT22	ISO_CLK_1V8	IO_L13P_T2L_N0_GC_QBC_64	1.8 (LVCMOS18)
AK39	MGT_PROGCLK_0_PIN_N	MGTREFCLK0N_121	MGT REFCLK
AK38	MGT_PROGCLK_0_PIN_P	MGTREFCLK0P_121	MGT REFCLK
R8	MGT_PROGCLK_1_PIN_N	MGTREFCLK0N_232	MGT REFCLK
R9	MGT_PROGCLK_1_PIN_P	MGTREFCLK0P_232	MGT REFCLK
V39	MGT_PROGCLK_2_PIN_N	MGTREFCLK0N_126	MGT REFCLK
V38	MGT_PROGCLK_2_PIN_P	MGTREFCLK0P_126	MGT REFCLK
AJ8	PCIE_LCL_REFCLK_PIN_N	MGTREFCLK1N_225	MGT REFCLK
AJ9	PCIE_LCL_REFCLK_PIN_P	MGTREFCLK1P_225	MGT REFCLK
AC8	PCIE_REFCLK_PIN_N	MGTREFCLK0N_227	MGT REFCLK
AC9	PCIE_REFCLK_PIN_P	MGTREFCLK0P_227	MGT REFCLK

Table 8 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	Bank Voltage
AA3	PCIE_RX0_N	MGTYRXN3_227	MGT
AA4	PCIE_RX0_P	MGTYRXP3_227	MGT
AB1	PCIE_RX1_N	MGTYRXN2_227	MGT
AB2	PCIE_RX1_P	MGTYRXP2_227	MGT
AC3	PCIE_RX2_N	MGTYRXN1_227	MGT
AC4	PCIE_RX2_P	MGTYRXP1_227	MGT
AD1	PCIE_RX3_N	MGTYRXN0_227	MGT
AD2	PCIE_RX3_P	MGTYRXP0_227	MGT
AE3	PCIE_RX4_N	MGTYRXN3_226	MGT
AE4	PCIE_RX4_P	MGTYRXP3_226	MGT
AF1	PCIE_RX5_N	MGTYRXN2_226	MGT
AF2	PCIE_RX5_P	MGTYRXP2_226	MGT
AG3	PCIE_RX6_N	MGTYRXN1_226	MGT
AG4	PCIE_RX6_P	MGTYRXP1_226	MGT
AH1	PCIE_RX7_N	MGTYRXN0_226	MGT
AH2	PCIE_RX7_P	MGTYRXP0_226	MGT
Y6	PCIE_TX0_PIN_N	MGTYTXN3_227	MGT
Y7	PCIE_TX0_PIN_P	MGTYTXP3_227	MGT
AB6	PCIE_TX1_PIN_N	MGTYTXN2_227	MGT
AB7	PCIE_TX1_PIN_P	MGTYTXP2_227	MGT
AD6	PCIE_TX2_PIN_N	MGTYTXN1_227	MGT
AD7	PCIE_TX2_PIN_P	MGTYTXP1_227	MGT
AF6	PCIE_TX3_PIN_N	MGTYTXN0_227	MGT
AF7	PCIE_TX3_PIN_P	MGTYTXP0_227	MGT
AH6	PCIE_TX4_PIN_N	MGTYTXN3_226	MGT
AH7	PCIE_TX4_PIN_P	MGTYTXP3_226	MGT
AK6	PCIE_TX5_PIN_N	MGTYTXN2_226	MGT
AK7	PCIE_TX5_PIN_P	MGTYTXP2_226	MGT
AM6	PCIE_TX6_PIN_N	MGTYTXN1_226	MGT
AM7	PCIE_TX6_PIN_P	MGTYTXP1_226	MGT
AN4	PCIE_TX7_PIN_N	MGTYTXN0_226	MGT
AN5	PCIE_TX7_PIN_P	MGTYTXP0_226	MGT
AM17	PERST0_1V8_L	IO_T3U_N12_PERSTN0_65	1.8 (LVCMOS18)
AH11	PROGRAM_B_1V8	PROGRAM_B_0	1.8 (LVCMOS18)
T23	QSFP_0_INT_1V8_L	IO_L6P_T0U_N10_AD6P_72	1.8 (LVCMOS18)
P22	QSFP_0_LPMODE_1V8	IO_L5N_T0U_N9_AD14N_72	1.8 (LVCMOS18)

Table 8 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	Bank Voltage
P20	QSFP_0_MODPRS_L	IO_L1P_T0L_N0_DBC_72	1.8 (LVCMOS18)
R22	QSFP_0_RST_1V8_L	IO_L5P_T0U_N8_AD14P_72	1.8 (LVCMOS18)
BC46	QSFP_0_RX0_N	MGTYRXN0_120	MGT
BC45	QSFP_0_RX0_P	MGTYRXP0_120	MGT
BA46	QSFP_0_RX1_N	MGTYRXN1_120	MGT
BA45	QSFP_0_RX1_P	MGTYRXP1_120	MGT
AW46	QSFP_0_RX2_N	MGTYRXN2_120	MGT
AW45	QSFP_0_RX2_P	MGTYRXP2_120	MGT
AU46	QSFP_0_RX3_N	MGTYRXN3_120	MGT
AU45	QSFP_0_RX3_P	MGTYRXP3_120	MGT
K1	QSFP_0_RX4_N	MGTYRXN0_233	MGT
K2	QSFP_0_RX4_P	MGTYRXP0_233	MGT
H1	QSFP_0_RX5_N	MGTYRXN1_233	MGT
H2	QSFP_0_RX5_P	MGTYRXP1_233	MGT
F1	QSFP_0_RX6_N	MGTYRXN2_233	MGT
F2	QSFP_0_RX6_P	MGTYRXP2_233	MGT
D1	QSFP_0_RX7_N	MGTYRXN3_233	MGT
D2	QSFP_0_RX7_P	MGTYRXP3_233	MGT
N22	QSFP_0_SCL_1V8	IO_L4P_T0U_N6_DBC_AD7P_72	1.8 (LVCMOS18)
M22	QSFP_0_SDA_1V8	IO_L4N_T0U_N7_DBC_AD7N_72	1.8 (LVCMOS18)
BD43	QSFP_0_TX0_N	MGTYTXN0_120	MGT
BD42	QSFP_0_TX0_P	MGTYTXP0_120	MGT
BB43	QSFP_0_TX1_N	MGTYTXN1_120	MGT
BB42	QSFP_0_TX1_P	MGTYTXP1_120	MGT
AY43	QSFP_0_TX2_N	MGTYTXN2_120	MGT
AY42	QSFP_0_TX2_P	MGTYTXP2_120	MGT
AV43	QSFP_0_TX3_N	MGTYTXN3_120	MGT
AV42	QSFP_0_TX3_P	MGTYTXP3_120	MGT
G4	QSFP_0_TX4_N	MGTYTXN0_233	MGT
G5	QSFP_0_TX4_P	MGTYTXP0_233	MGT
F6	QSFP_0_TX5_N	MGTYTXN1_233	MGT
F7	QSFP_0_TX5_P	MGTYTXP1_233	MGT
E4	QSFP_0_TX6_N	MGTYTXN2_233	MGT
E5	QSFP_0_TX6_P	MGTYTXP2_233	MGT
C4	QSFP_0_TX7_N	MGTYTXN3_233	MGT
C5	QSFP_0_TX7_P	MGTYTXP3_233	MGT

Table 8 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	Bank Voltage
K24	QSFP_1_INT_1V8_L	IO_L8P_T1L_N2_AD5P_72	1.8 (LVCMOS18)
K23	QSFP_1_LPMODE_1V8	IO_L7N_T1L_N1_QBC_AD13N_72	1.8 (LVCMOS18)
N20	QSFP_1_MODPRS_L	IO_L1N_T0L_N1_DBC_72	1.8 (LVCMOS18)
L23	QSFP_1_RST_1V8_L	IO_L7P_T1L_N0_QBC_AD13P_72	1.8 (LVCMOS18)
AR46	QSFP_1_RX0_N	MGTYRXN0_121	MGT
AR45	QSFP_1_RX0_P	MGTYRXP0_121	MGT
AN46	QSFP_1_RX1_N	MGTYRXN1_121	MGT
AN45	QSFP_1_RX1_P	MGTYRXP1_121	MGT
AL46	QSFP_1_RX2_N	MGTYRXN2_121	MGT
AL45	QSFP_1_RX2_P	MGTYRXP2_121	MGT
AJ46	QSFP_1_RX3_N	MGTYRXN3_121	MGT
AJ45	QSFP_1_RX3_P	MGTYRXP3_121	MGT
T1	QSFP_1_RX4_N	MGTYRXN0_232	MGT
T2	QSFP_1_RX4_P	MGTYRXP0_232	MGT
R3	QSFP_1_RX5_N	MGTYRXN1_232	MGT
R4	QSFP_1_RX5_P	MGTYRXP1_232	MGT
P1	QSFP_1_RX6_N	MGTYRXN2_232	MGT
P2	QSFP_1_RX6_P	MGTYRXP2_232	MGT
M1	QSFP_1_RX7_N	MGTYRXN3_232	MGT
M2	QSFP_1_RX7_P	MGTYRXP3_232	MGT
R23	QSFP_1_SCL_1V8	IO_L6N_T0U_N11_AD6N_72	1.8 (LVCMOS18)
T21	QSFP_1_SDA_1V8	IO_T0U_N12_VRP_72	1.8 (LVCMOS18)
AT43	QSFP_1_TX0_N	MGTYTXN0_121	MGT
AT42	QSFP_1_TX0_P	MGTYTXP0_121	MGT
AP43	QSFP_1_TX1_N	MGTYTXN1_121	MGT
AP42	QSFP_1_TX1_P	MGTYTXP1_121	MGT
AM43	QSFP_1_TX2_N	MGTYTXN2_121	MGT
AM42	QSFP_1_TX2_P	MGTYTXP2_121	MGT
AL41	QSFP_1_TX3_N	MGTYTXN3_121	MGT
AL40	QSFP_1_TX3_P	MGTYTXP3_121	MGT
L4	QSFP_1_TX4_N	MGTYTXN0_232	MGT
L5	QSFP_1_TX4_P	MGTYTXP0_232	MGT
K6	QSFP_1_TX5_N	MGTYTXN1_232	MGT
K7	QSFP_1_TX5_P	MGTYTXP1_232	MGT
J4	QSFP_1_TX6_N	MGTYTXN2_232	MGT
J5	QSFP_1_TX6_P	MGTYTXP2_232	MGT

Table 8 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	Bank Voltage
H6	QSFP_1_TX7_N	MGTYTXN3_232	MGT
H7	QSFP_1_TX7_P	MGTYTXP3_232	MGT
J20	QSFP_2_INT_1V8_L	IO_T1U_N12_72	1.8 (LVCMOS18)
J22	QSFP_2_LPMODE_1V8	IO_L12N_T1U_N11_GC_72	1.8 (LVCMOS18)
M23	QSFP_2_MODPRS_L	IO_L2N_T0L_N3_72	1.8 (LVCMOS18)
K22	QSFP_2_RST_1V8_L	IO_L12P_T1U_N10_GC_72	1.8 (LVCMOS18)
W46	QSFP_2_RX0_N	MGTYRXN0_126	MGT
W45	QSFP_2_RX0_P	MGTYRXP0_126	MGT
U46	QSFP_2_RX1_N	MGTYRXN1_126	MGT
U45	QSFP_2_RX1_P	MGTYRXP1_126	MGT
R46	QSFP_2_RX2_N	MGTYRXN2_126	MGT
R45	QSFP_2_RX2_P	MGTYRXP2_126	MGT
N46	QSFP_2_RX3_N	MGTYRXN3_126	MGT
N45	QSFP_2_RX3_P	MGTYRXP3_126	MGT
L46	QSFP_2_RX4_N	MGTYRXN0_127	MGT
L45	QSFP_2_RX4_P	MGTYRXP0_127	MGT
J46	QSFP_2_RX5_N	MGTYRXN1_127	MGT
J45	QSFP_2_RX5_P	MGTYRXP1_127	MGT
G46	QSFP_2_RX6_N	MGTYRXN2_127	MGT
G45	QSFP_2_RX6_P	MGTYRXP2_127	MGT
E46	QSFP_2_RX7_N	MGTYRXN3_127	MGT
E45	QSFP_2_RX7_P	MGTYRXP3_127	MGT
K21	QSFP_2_SCL_1V8	IO_L11P_T1U_N8_GC_72	1.8 (LVCMOS18)
J21	QSFP_2_SDA_1V8	IO_L11N_T1U_N9_GC_72	1.8 (LVCMOS18)
T43	QSFP_2_TX0_N	MGTYTXN0_126	MGT
T42	QSFP_2_TX0_P	MGTYTXP0_126	MGT
P43	QSFP_2_TX1_N	MGTYTXN1_126	MGT
P42	QSFP_2_TX1_P	MGTYTXP1_126	MGT
M43	QSFP_2_TX2_N	MGTYTXN2_126	MGT
M42	QSFP_2_TX2_P	MGTYTXP2_126	MGT
K43	QSFP_2_TX3_N	MGTYTXN3_126	MGT
K42	QSFP_2_TX3_P	MGTYTXP3_126	MGT
H43	QSFP_2_TX4_N	MGTYTXN0_127	MGT
H42	QSFP_2_TX4_P	MGTYTXP0_127	MGT
F43	QSFP_2_TX5_N	MGTYTXN1_127	MGT
F42	QSFP_2_TX5_P	MGTYTXP1_127	MGT

Table 8 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	Bank Voltage
D43	QSFP_2_TX6_N	MGTYTXN2_127	MGT
D42	QSFP_2_TX6_P	MGTYTXP2_127	MGT
B43	QSFP_2_TX7_N	MGTYTXN3_127	MGT
B42	QSFP_2_TX7_P	MGTYTXP3_127	MGT
L20	QSFP_3_INT_1V8_L	IO_L10N_T1U_N7_QBC_AD4N_72	1.8 (LVCMOS18)
M20	QSFP_3_LPMODE_1V8	IO_L10P_T1U_N6_QBC_AD4P_72	1.8 (LVCMOS18)
N23	QSFP_3_MODPRS_L	IO_L2P_T0L_N2_72	1.8 (LVCMOS18)
L21	QSFP_3_RST_1V8_L	IO_L9N_T1L_N5_AD12N_72	1.8 (LVCMOS18)
AG46	QSFP_3_RX0_N	MGTYRXN0_122	MGT
AG45	QSFP_3_RX0_P	MGTYRXP0_122	MGT
AF44	QSFP_3_RX1_N	MGTYRXN1_122	MGT
AF43	QSFP_3_RX1_P	MGTYRXP1_122	MGT
AE46	QSFP_3_RX2_N	MGTYRXN2_122	MGT
AE45	QSFP_3_RX2_P	MGTYRXP2_122	MGT
AD44	QSFP_3_RX3_N	MGTYRXN3_122	MGT
AD43	QSFP_3_RX3_P	MGTYRXP3_122	MGT
AC46	QSFP_3_RX4_N	MGTYRXN0_125	MGT
AC45	QSFP_3_RX4_P	MGTYRXP0_125	MGT
AB44	QSFP_3_RX5_N	MGTYRXN1_125	MGT
AB43	QSFP_3_RX5_P	MGTYRXP1_125	MGT
AA46	QSFP_3_RX6_N	MGTYRXN2_125	MGT
AA45	QSFP_3_RX6_P	MGTYRXP2_125	MGT
Y44	QSFP_3_RX7_N	MGTYRXN3_125	MGT
Y43	QSFP_3_RX7_P	MGTYRXP3_125	MGT
J24	QSFP_3_SCL_1V8	IO_L8N_T1L_N3_AD5N_72	1.8 (LVCMOS18)
M21	QSFP_3_SDA_1V8	IO_L9P_T1L_N4_AD12P_72	1.8 (LVCMOS18)
AK43	QSFP_3_TX0_N	MGTYTXN0_122	MGT
AK42	QSFP_3_TX0_P	MGTYTXP0_122	MGT
AJ41	QSFP_3_TX1_N	MGTYTXN1_122	MGT
AJ40	QSFP_3_TX1_P	MGTYTXP1_122	MGT
AG41	QSFP_3_TX2_N	MGTYTXN2_122	MGT
AG40	QSFP_3_TX2_P	MGTYTXP2_122	MGT
AE41	QSFP_3_TX3_N	MGTYTXN3_122	MGT
AE40	QSFP_3_TX3_P	MGTYTXP3_122	MGT
AC41	QSFP_3_TX4_N	MGTYTXN0_125	MGT
AC40	QSFP_3_TX4_P	MGTYTXP0_125	MGT

Table 8 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	Bank Voltage
AA41	QSFP_3_TX5_N	MGTYTXN1_125	MGT
AA40	QSFP_3_TX5_P	MGTYTXP1_125	MGT
W41	QSFP_3_TX6_N	MGTYTXN2_125	MGT
W40	QSFP_3_TX6_P	MGTYTXP2_125	MGT
U41	QSFP_3_TX7_N	MGTYTXN3_125	MGT
U40	QSFP_3_TX7_P	MGTYTXP3_125	MGT
BC15	RF_DIR	IO_L21P_T3L_N4_AD8P_66	1.8 (LVCMOS18)
BB9	RF_IO	IO_L14P_T2L_N2_GC_66	1.8 (LVCMOS18)
AH39	SI5328_0_OUT_0_PIN_N	MGTREFCLK1N_121	MGT REFCLK
AH38	SI5328_0_OUT_0_PIN_P	MGTREFCLK1P_121	MGT REFCLK
N8	SI5328_0_OUT_1_PIN_N	MGTREFCLK1N_232	MGT REFCLK
N9	SI5328_0_OUT_1_PIN_P	MGTREFCLK1P_232	MGT REFCLK
AY23	SI5328_0_REFCLK_IN_N	IO_L11N_T1U_N9_GC_64	1.8 (LVDS)
AY24	SI5328_0_REFCLK_IN_P	IO_L11P_T1U_N8_GC_64	1.8 (LVDS)
AL24	SI5328_0_RST_1V8_L	IO_L24P_T3U_N10_64	1.8 (LVCMOS18)
T39	SI5328_1_OUT_0_PIN_N	MGTREFCLK1N_126	MGT REFCLK
T38	SI5328_1_OUT_0_PIN_P	MGTREFCLK1P_126	MGT REFCLK
AN8	SI5328_1_OUT_1_PIN_N	MGTREFCLK1N_224	MGT REFCLK
AN9	SI5328_1_OUT_1_PIN_P	MGTREFCLK1P_224	MGT REFCLK
AW22	SI5328_1_REFCLK_IN_N	IO_L12N_T1U_N11_GC_64	1.8 (LVDS)
AW23	SI5328_1_REFCLK_IN_P	IO_L12P_T1U_N10_GC_64	1.8 (LVDS)
AM24	SI5328_1_RST_1V8_L	IO_L24N_T3U_N11_64	1.8 (LVCMOS18)
AM21	SI5328_1V8_SCL	IO_L23N_T3U_N9_64	1.8 (LVCMOS18)
AL21	SI5328_1V8_SDA	IO_L23P_T3U_N8_64	1.8 (LVCMOS18)
BF14	SPARE_SCL	IO_L5N_T0U_N9_AD14N_66	1.8 (LVCMOS18)
BE15	SPARE_SDA	IO_L6P_T0U_N10_AD6P_66	1.8 (LVCMOS18)
BF15	SPARE_WP	IO_L6N_T0U_N11_AD6N_66	1.8 (LVCMOS18)
BC11	SRVC_MD_L_1V8	IO_L3P_T0L_N4_AD15P_66	1.8 (LVCMOS18)
AV9	USER_LED_G0_1V8	IO_L16P_T2U_N6_QBC_AD3P_66	1.8 (LVCMOS18)
AV8	USER_LED_G1_1V8	IO_L16N_T2U_N7_QBC_AD3N_66	1.8 (LVCMOS18)
AY8	USER_LED_G2_1V8	IO_L17P_T2U_N8_AD10P_66	1.8 (LVCMOS18)
AY7	USER_LED_G3_1V8	IO_L17N_T2U_N9_AD10N_66	1.8 (LVCMOS18)
AW8	USER_LED_G4_1V8	IO_L18P_T2U_N10_AD2P_66	1.8 (LVCMOS18)
AW7	USER_LED_G5_1V8	IO_L18N_T2U_N11_AD2N_66	1.8 (LVCMOS18)
BA15	USR_SW_0	IO_L22N_T3U_N7_DBC_AD0N_66	1.8 (LVCMOS18)
BA14	USR_SW_1	IO_L23P_T3U_N8_66	1.8 (LVCMOS18)

Table 8 : Complete Pinout Table

Revision History

Date	Revision	Changed By	Nature of Change
29 Aug 2019	1.0	K. Roth	Initial Release
8 Nov 2019	1.1	K. Roth	Updated sections Power Requirements and Switches to detail 12V auto-detect feature for rev2 boards.
18 Feb 2020	1.2	K. Roth	Added section KN32 – Emissions
30 Apr 2020	1.3	K. Roth	Image QSFP-DD Location updated to show proper QSFP cage order at previous revision 1.2, and modified section Si5328 to remove reference to VCU110 and added notes on RXOUTCLK.
12 Jun 2020	1.4	K. Roth	Image OpenCAPI Pinout added to show J10 pinout, and updated Thermal Performance with detailed data for blower and LFM thermal performance.
17 Jul 2023	1.5	K. Roth	Separated PCB dimensions in Physical Specifications for consistency with other user guides.

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